ABSTRACT OF THE DISCLOSURE

The present invention relates to a nonvolatile memory device having asymmetric source/drain regions and a fabricating method thereof. In the device, a first and second impurity regions are formed in a substrate, and are separated by a first channel region and a second channel region. A tunnel insulating layer, a charge storing layer, and a gate interlayer insulating layer is disposed on the substrate in the first channel region, with the gate interlayer insulating layer being extended over the substrate in the second channel region. A control gate is then disposed over the previously formed layers in both regions. The first channel region and the first impurity region are, respectively, wider than the second channel region and the second impurity region. Thus, the erase speed of the device can be increased in an erase operation, by allowing an increased hot-hole injection rate.